AMENDMENTS TO THE DRAWINGS

The attached sheet of Patent Drawings including Figs. 1-5, replaces a sheet of Drawings including Figs. 1 and 2 of the original Drawings, a sheet which includes Figs. 3 and 4 of the original Drawings, and a sheet which includes Fig. 5 of the original Drawings.

Attachment: Replacement sheet of Patent Drawings, including Figs. 1-5.

REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Official Action dated 3 June 2005. Responsive to the rejections and objections to the Claims in the Official Action, Claims 1, 2, 5, 6, 9, 11, 12, 16, and 19 have been amended.

In the Official Action, original Drawings were objected to under 37 C.F.R. § 1.83(a) as not agreeable with the Specification. Accordingly, the original Drawing Figs. 1-5 have been replaced with the new Figs. 1-5 of the Patent Drawings. These new Figs. 1-5 show all claimed features of the invention and the original Specification has antecedent basis for these newly introduced Figs. 1-5. No new matter has been entered by replacement of the Drawings.

In the Official Action, Claims 2 and 12 were objected to under 37 C.F.R. 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous Claim. Claims 2 and 12 have been amended to overcome the 37 C.F.R. § 1.75(c) objection.

Further, Claims 9 and 19 were objected to due to minor informalities. Accordingly, Claims 9 and 19 have been amended to obviate the objection.

Claims 1-20 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Particularly, Claims 1, 5, 6, 11, and 16 were found to have insufficient antecedent basis for the limitation "said channel".

Accordingly, Claims 1, 5, 6, 11, and 16 have been amended to replace the language "said channel" with -- said at least one channel -- , as was suggested by the Examiner.

In the Official Action, the Examiner rejected Claims 1, 2, 7, and 10 under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al., U.S. Patent #3,956,052 in view of Mizuno, et al., U.S. Patent #5,466,325; Claims 3 and 4 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al., in view of Mizuno, et al., and further in view of Zhao, et al., U.S. Patent #6,245,663; Claims 5 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al., in view of Mizuno, et al., and further in view of Hayama, et al., U.S. Patent #6,378,424; Claims 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al. in view of Mizuno, et al., and further in view of Schreiber, et al., U.S. Patent #5,233,157; Claims 11, 12, 16, 17, and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al., in view of Mizuno, et al., and Hayama, et al.; Claims 13 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al., in view of Mizuno, et al., and Hayama, et al., and further in view of Zhao, et al.; Claim 15 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al. in view of Mizuno, et al., and Hayama, et al., and further in view of Ellis, U.S. Patent #3,923,697; Claims 18 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Koste, et al. in view of Mizuno, et al., and Hayama, et al., and further in view of Schreiber, et al.

Responsive to the 35 U.S.C. § 103(a) rejections made in the Official Action, Independent Claims 1 and 11 have been amended to emphasize therein the features separating the present invention from the cited prior art taken singly or in combination.

Prior to consideration of the features distinguishing the present invention from the cited prior art, it is believed that a brief discussion of the invention in question is in order.

The present invention relates to forming of high resolution electronic circuits on a substrate. The method includes the deposition of a layer of dielectric film 14 on a substrate 12, laser drilling of the channels in the layer of dielectric film (channels 16), as well as in the substrate (channels 18), filling the channels formed in the layer of dielectric film and the substrate with a conductive material 20, and heating the thus created structure containing substrate, dielectric film, and electrically conductive material within the channels.

The heating (baking) which follows after the filling of channels 16 and 18 with the material 20, causes melting of the material 20 and setting it within channels 16 and 18. Depending on the composition of material 20, the volume of material 20 within the channels 16 and 18 may decrease during the baking process. Should this occur, an additional quantity of material 20 may be added to the channels 16 and 18 and heated (or baked) a second time.

This heating (baking) increases the strength of the material 20 and forms a strong bond between the material 20 and substrate 12 which is necessary for forming permanent electronic circuitry on the substrate 12.

Further, as shown in Fig. 4, a release layer 22 is laminated on an upper surface of the dielectric film layer 14 and filler material 20. Following the lamination of the release layer 22, the created structure including the substrate 12, the dielectric film 14, filler material 20 within the channels 16 and 18, and the release layer 22 is heated again in order to increase the adhesion between the adhesive on the release layer 22 and the dielectric film layer 14. This additional heating also enhances the mechanical integrity of the filler material 20 within the channels 16 and 18, and creates a permanent adhesion between the filler material 20 and the substrate 12. The heating of the substrate, thin dielectric film layer 14, filling material 20, and the release layer 22 is conducted at a temperature in a range approximately between 150°C and 175°C.

A final step of the novel method of the present invention is the peeling or otherwise removal of the release layer 22 from the substrate 12 and filling material 20. As shown in Fig. 5, since the dielectric film layer 14 adheres to the release layer 22, it is removed therealong. The filler material 20 permanently remains on the substrate 12 due to the heating of the filler material within the channels 16 and 18 which provides the material 20 with the enhanced mechanical integrity and permanent bonding to the top surface of the substrate 12.

Referring to the references cited by the Examiner, Koste, et al. is directed to a method of metallizing a ceramic sheet. A thin organic layer 10 is laminated on the top of a dielectric substrate 12. An energy beam 14 is employed to form a plurality of via interconnection holes 16 and recessed channels 18. In the subsequent metal filling step, a metal 26 fills in the vias 16 and channels 18. After the metal deposition, the layer 10 is peeled of the substrate 12, thus leaving the ceramic substrate 12 with recessed metallurgy deposited in interconnection vias 16 and channels 18.

It is respectfully submitted that Koste, et al. reference fails to suggest, disclose, or render obvious the method regarded by the Applicant as the invention. Specifically:

(A) Koste, et al., in contrast to the present invention, is silent on mechanically strengthening the filler material within the vias 16 and channels 18, and on improving adhesion between the filler material 26 and the substrate 12 by heating and baking the structure.

It is believed that since Koste, et al. method lacks the heating (or baking) step after the conductive material 22 is filled in the vias 16 and channels 18, the removal of the mask 22 from the substrate 12 may cause an unwanted disturbance of the conductive material in the vias 16 and the channels 18 which may disrupt the integrity of the conducting metallurgy in the vias 16 and the channel 18, thus undesirably reducing the yield of the manufactured devices of Koste, et al.

In the present invention, the structure containing the filling material 20 within the channels 16 and 18 is heated so that the filling material 20 acquires an enhanced mechanical material integrity and adheres to the upper surface of the substrate in substantially permanent fashion in order to remain permanently on the substrate 12 when the dielectric layer 14 and the release layer 22 are removed from the substrate 12.

It is due to sufficient heating of the filler material 20 in the present invention, by which high integrity of the filler material 20 within the channels 16 and 18 is achieved. Additionally a permanent bond is created between the filler material 20 and the top surface of the substrate 12. Peeling of the dielectric layer 14 along with the layer 22 will not cause a destruction of the filler material 20 within the channels 18 and 16, nor it will cause removal of conductive structures from the substrate 12. Manufacturing of electronic devices in accordance with the method of the present invention therefore achieves high yield and improved quality of the circuitry created and permanently remaining on the substrate.

(B) In Koste, et al., the mask 22 is peeled from the substrate 12 without the help of any additional release layer which may be glued on the top thereof.

Opposingly in the present invention, the release layer 22 is laminated on the top of the dielectric layer 14, and by peeling the laminate release layer 22, the dielectric layer adhered thereto is concurrently removed.

Mizuno, et al., another reference cited by the Examiner, is directed to a photoresist removing method for removing a photoresist pattern formed on a semiconductor wafer. The method comprises adhering an adhesive tape 6 on the upper surface of a resist pattern 4 formed on the article and removal of the resist pattern together with the adhesive tape 6.

(A) It is respectfully submitted that in the Mizuno, et al. reference, in contradistinction with the present invention, only a photoresist pattern exists on the wafer and no filler material exists between the photoresist elements 4. When the tape 6 adheres to the photoresist 4, it is not Mizuno, et al.'s concern that such may remove other structures existing on the wafer in addition to the photoresist, since these additional elements simply do not exist thereon. Therefore, Mizuno, et al. is not concerned with selective removal of photoresist 4 while leaving other structures on the substrate. Therefore, as Mizuno, et al. is not concerned with such a problem, this reference is not intended for, and thus is silent on enhancing integrity of any structure on the wafer or on creation of a permanent adhesion between structures on the wafer and the wafer itself. Moreover, it is clear that in Mizuno, et al., it would be very undesirable to enhance bonding between the elements on the wafer and the wafer, since the goal of Mizuno, et al. is to easily remove these structures from the wafer, and not to permanently retain them thereon.

While the major concern of the present invention is to guarantee that the filler material 20 permanently remains on the substrate 12 and is not removed by peeling the release layer 22 along with the dielectric layer 14 from the substrate. Due to baking and heating in the method of the present invention, the filler material 20 within the channels 16 and 18 acquires an enhanced integrity and is permanently adhered to the substrate 12 so that the removal of the release tape 12 and dielectric layer 14 cannot remove the conductive structures 20 from the surface of the substrate.

(B) Mizuno, et al. reference does have a step B which is an adhesion strengthening step. This step however is intended exclusively for adhering the tape 6 to the top surface of the photoresist 4, and not to bond a resist 4 to the wafer. Additionally, Mizuno, et al. is silent on exact temperature parameters of the adhesion strengthening step thereof.

In the present invention, the bond between the release layer 22 and the layer 14 is enhanced by adhesion strengthening step, however, the step is carried out in a specific temperature range, particularly in the temperature range between 150° and 175°C. This heating step creates permanent bonds between the conductive structures 20 and the substrate, as well as enhancing the integrity of the conductive structures 20. It is respectfully noted that these features are completely missing in Mizuno, et al.

Neither Koste, et al., nor Mizuno, et al. taken singly or in combination, include heating of the substrate and electrically conductive material to a temperature in the range

of approximately 150°C - 175°C to enhance mechanical integrity of the conductive material within the channels and to create permanent adhesion between the conductive material and the upper surface of the substrate. Claim 1 as amended includes this feature, and therefore, is believed to be patentably distinct over the Koste, et al. and Mizuno, et al., taken singly or in combination thereof. Accordingly, it is believed that Claim 1 as amended shows patentable distinction over the combination of references cited.

Hayama, et al., another reference cited by the Examiner, in rejection of Independent Claim 11 if taken in combination with Koste, et al. and Mizuno, et al., describes a method of fabricating electronic parts which is capable of forming fine patterns with some accuracy. In Hayama, et al., an intaglio plate 20 which has grooves 21 and 22, are filled with the silver paste 24. Upon filling the grooves 21 and 22 with the conductive paste 24, the drying step is performed which consists of two stages, a first stage of pre-drying at a temperature of 100°C or less for five minutes, and a second stage of drying at a temperature of 150°C for five minutes. Alternatively, the drying step is performed by raising the temperature from room temperature to 150°C with a moderate increase rate of 15°C per minute.

Prior to filling the grooves 21 and 22 in the substrate 20 with the silver paste 24, a release layer 23 is formed within the grooves and on the surface of the substrate 20, on the top of which the silver paste 24 is deposited.

Next, a thermoplastic resin layer 28 is formed on an insulating substrate 2, thereby obtaining an object onto which the conductor pattern is transferred. The thermoplastic resin layer 28 functions as an adhesive layer when the conductor pattern 24 is transferred thereon.

As shown in Fig. 6 of Hayama, et al. reference, the substrate 20 and the insulating substrate 2 are laminated together so that the surface of the plate 20, on which the grooves 21 and 22 filled with the silver paste are formed, and the thermoplastic resin layer face each other. The temperature during the laminating step is set in the range from a temperature lower than the glass transition temperature of the used thermoplastic resin layer 28 by 30°C to one higher than that by 100°C. If the laminated temperature is higher than the upper limit described above, the silver paste 24 does not transfer well from the grooves 21 and 22 of the plate 20. This is due to the fact that the thermoplastic resin layer 28 has too much fluidity at the temperature above the upper limit, and therefore, the thermoplastic resin layer 28 is thinned by the pressure applied during lamination.

On the other hand, if the laminating temperature is lower than the lower limit described above, the silver paste 24 will not transfer well from the grooves 21 and 22 of the plate 20. This is due to the fact that the thermoplastic resin layer 28 does not have sufficient fluidity at the temperature below the lower limit, and therefore, the silver paste 24 and the thermoplastic resin layer 28 are not sufficiently attached each to the other. Therefore, the plate 20 filled with the silver paste 24 and the insulating substrate 2 on

which the PVB layer 28 is formed are laminated together below a temperature of 100°C using thermal rollers.

The transfer step is conducted as shown in Fig. 8. The temperature of the laminated plate 20 and the insulating substrate 2 is lowered to room temperature, and the plate 20 is peeled from the insulating substrate 2 thereby transferring the patterned silver paste 24 onto the substrate 2.

(A). It is respectfully submitted that the Hayama method is quite distant from the method of the present invention, and as a matter of fact, represents a reverse process in which the conductive pattern does not remain on the substrate where it is formed but is transferred.

In contradistinction to Hayama, et al. Patent, in the method of the present invention, the conductive pattern permanently remains on the substrate where it is formed. No transferring of the conductive pattern to another structure is intended or contemplated in the present invention.

(B). In Hayama, et al., the maximum temperature which the structure is subjected to is 100°C (Column 9, Line 55) since at a higher temperature, the silver paste 24 does not transfer well from the grooves 21 and 22 of the plate 20 to the substrate 2. This is due to the fact that the thermoplastic resin layer 28 has too much fluidity at the temperature above 100°C (Column 9, Lines 15-25).

In contradistinction to Hayama, et al., in the present invention, in order to provide the best adhesion characteristics of the filler material 20 to the substrate, the structure including substrate 12, the dielectric layer 14, the filler material 20, and the release layer 22, is heated to the temperature in the range between 150°C and 175°C. In this temperature region, the process of Hayama, et al. cannot be fulfilled as intended, as the transferred structures 24 cannot adhere to the substrate 2 since the layer 28 loses its adhesive qualities.

(C). In Hayama, et al., after the grooves 21 and 22 in the plate 20 are filled with the silver paste 24, the structure is dried in the drying step 240 which consists of two stages: a first stage of pre-drying at a temperature of 100°C or less for five minutes, and a second stage of drying at a temperature of 150°C for five minutes. Alternatively, the drying step may be conducted by raising the temperature from room temperature to 150°C.

In contradistinction to Hayama, et al., where the maximum temperature is 150°C, in the present invention, the heating process is performed starting at 150°C and rises to 175°C.

It is clear therefore that the Hayama, et al. Patent does not suggest, disclose, or render obvious the heating of the substrate, dielectric film, electrically conductive material in a channel and a release layer to a temperature in a range of approximately 150°C - 175°C to create permanent adhesion between the conductive material and the

upper surface of the substrate so that the conductive pattern 20 remains permanently on the substrate where it is formed. The Hayama, et al. Patent teaches away from creating permanent bonds between the conductive pattern and the substrate where it is formed, since Kayama, et al. does not keep the conductive pattern on the substrate where it is created. It is further noted that under the temperature regime of the present invention, Hayama, et al. method cannot be operable for its purposes and objectives.

It is believed that none of the references cited by the Examiner in the rejection of Independent Claim 11, e.g., Koste, et al., Mizuno, et al., and Hayama, et al., taken singly or in combination, include:

"...heating said substrate, said layer of dielectric film, said electrically conductive material in said at least one channel, and said release layer to a temperature in a range of approximately 150°C - 175°C to enhance mechanical integrity of said conductive material within said at lest one channel and to create permanent adhesion between said conductive material and said upper surface of said substrate..." and

"...conductive material formed, patterned, and remaining permanently on said upper surface of said substrate".

Claim 11, as amended, includes this feature, completely missing in the cited prior art, and therefore is believed to be patentably distinct over Koste, et al., Mizuno, et al., and Hayama, et al., taken singly or in combination thereof. Accordingly, the allowance of Claim 11 is respectfully requested.

Zhao, et al., another reference cited by the Examiner, is directed to IC interconnect structures and manufacturing the same and was cited by the Examiner merely to show that conducting lines can be formed from silver or copper. This reference is however very distinct from the method of the present invention, and in contradistinction thereto, fails to teach laser milling of channels in the laminate dielectric layer on the top of the surface and the substrate, filling the channels with the conducting filler and heating it to provide enhanced mechanical integrity of the filler material in the channels and to form bonds between the filler material and the substrate, or to laminate a release layer on the top of the dielectric layer and peeling the release layer along with the dielectric layer to leave the conductive pattern permanently on the surface of the substrate.

Schreiber, et al., is a reference cited by the Examiner in rejection of Claims 8, 9, as well as Claims 18 and 19, as using an excimer laser operating in ultraviolet range, and disclosing a dielectric substrate formed from a polyimide.

Schreiber, et al. teaches a method for laser pattern ablation of fine circuitry elements or a stainless steel substrate 32 coated with a dielectric layer 34. An excimer laser projects a fine spot 40 upon the Teflon layer 34 with a power sufficient to ablate the Teflon 34 entirely through to the stainless steel substrate 32. A pattern of conductor material 70 is then plated upon the substrate 32 to fill the opening 40, and a dielectric substrate 76 made of polyimide is laminated upon the mandrel and upon the conductor

pattern. As a final stage, the dielectric substrate 76 together with the conductors 70 adhering thereto is separated from the substrate 32.

It is respectfully submitted that Schreiber, et al. Patent, similar to Hayama, et al. reference, in contradistinction to the method of the present invention, represents a process which is reverse to the process of the present invention. Particularly:

(A). In the present invention, the substrate on which the conductive pattern 20 is formed and permanently remains as the electronic circuit is the polyimide substrate 12.

While in Schreiber, et al., the conducting pattern 70 is formed on a stainless steel substrate 32.

(B). In contrast to Schreiber, et al., the method of the present invention is overly concerned with permanent adhesion of the conductive pattern 20 to the substrate 12 which is attained by heating the structure which includes the substrate 12 and the conductive material 20 formed thereon to provide such a permanent adhesion in order to guarantee that the conductive material 20 permanently remains on the substrate 12 on which it was created and to withstand peeling of the dielectric layer 14 and the release layer 22.

However, in Schreiber, et al., the conductive pattern 70 does not remain on the substrate 32 on which it was formed but is transferred to an additional substrate 76 in the transfer step which is a core step underlining the Schreiber, et al. method.

Schreiber, et al., in contrast to the present invention, not only is "not" concerned with providing an enhanced adhesion between the conductors 70 and the substrate 32 on which the conductive pattern is formed, but clearly teaches away from this concept.

(C) In Schreiber, et al., the method does contemplate a heating procedure during the lamination of the dielectric substrate 76 on the top of the substrate 32 and the plated conductors 70. This procedure however promotes bonding of conductors 70 to the substrate 76 which is laminated thereon, but not the bonding of the conductors 70 to the substrate 32 on which the pattern 70 is formed.

In contradistinction to the Schreiber, et al., the baking and heating of the material 20 on the substrate 12, is for promoting bonding between the conducting material 20 and the substrate 12, on which the conductive pattern was formed.

(D) In Schreiber, et al., the temperature at which the dielectric substrate 76 is laminated upon the substrate 32 and the conductors 70 formed thereon, is about 375°F (which is about 187.77°C). In Schreiber, et al., the temperature and pressure treatment during the lamination process is intended specifically for promoting bonding between the conductors 70 and the substrate 76 to which the conductors 70 are to be transferred.

In contradistinction to Schreiber, et al., the heating of the material 20 and the substrate 12 is performed at 150°C - 175°C to provide a permanent bonding between the material 20 and the substrate 12.

In the present invention, it is of importance that the conductive pattern 20 permanently remains on the substrate 12 and is not removed with the peeling of laminated dielectric layer 14 and release layer 22.

Therefore, Schreiber, et al. Patent, fails to suggest, disclose, or render obvious that the structure having the substrate 32, conductors 70, and the laminated substrate 2, is heated to a temperature in a range of 150°C - 175°C in order to create permanent adhesion between the conductive material and the upper surface of the substrate on which the conductive material is formed, patterned, and permanently remains.

Ellis, still another reference cited by the Examiner, in rejection of Claim 15 as showing heating by a radiant heat transfer, is directed to electrically conductive compositions suitable for the manufacture of coating compositions, heating elements, and structures which are useful where radiant, conductive, or convective heating is required.

It is respectfully submitted that citation of the Ellis Patent as the prior art for forming high resolution electronic circuits is directed to a reference believed to be quite remote from Applicant's concept, since the Ellis Patent pertains to the field of rather large installations such as wall panels, ceiling panels, underfloor converting coatings, baseboard heaters, etc., the sizes of which range in tens of square feet and square yards, and thus is very distant from the art of fabrication of miniature electronic structures such as high resolution electronic circuits of the present invention.

In Ellis, a conductive film is coated onto a panel and heated. No patterning is contemplated in Ellis for creation of high resolution electronic circuits on the substrate.

Opposingly, the present invention is a method for forming high resolution electronic circuits and is not concerned with films covering building material for rather large structures as used in construction of houses, etc.

It is respectfully submitted that even though Ellis shows radiant heating, the principles of Ellis cannot be merely automatically transferred to radiant heating of the conductive pattern formed on a wafer for production of high resolution electronic circuits.

The Examiner suggested the combination of Koste, et al. with Mizuno, et al. in rejection of Claims 1, 2, 7, and 10; the Examiner further rejected the Claims 3 and 4 based on combination of Koste, et al. in view of Mizuno, et al., and Zhao, et al.; the Claims 5 and 6 were rejected as being unpatentable over Koste, et al. in view of Mizuno, et al., and further in view of Hayama, et al.; Claims 8 and 9 were rejected over Koste, et al. in view of Mizuno, et al., and further in view of Schreiber, et al.; Claims 11, 12, 16, 17, and 20 were rejected as being unpatentable over Koste, et al. in view of Mizuno, et al., and Hayama, et al.; Claims 13 and 14 were rejected in view of Koste, et al. and Mizuno, et al., as well as Hayama, et al., and further in view of Zhao, et al.; Claim 15 was rejected based on Koste, et al. in view of Mizuno, et al. and Hayama, et al. and further in

view of Ellis; and Claims 18 and 19 were rejected based on Koste, et al. in view of Mizuno, et al. and Hayama, et al., and further in view of Schreiber, et al.

Absent Applicant's disclosure, there is no motivation for combining the prior art references as suggested by the Examiner. It can only be thought of as an improper use of "hindsight", using Applicant's disclosure as a "blueprint" for the combination, that the Examiner suggests such a combination of references, as presented above.

Arguendo, even if the teachings of the prior art references, as suggested by the Examiner, or even in any other combinations thereof, are combined, it is believed that the combination of elements of the invention of the subject Patent Application, as now claimed, in Independent Claims 1 and 11, provides patentable distinction over the method resulting from the Examiner's suggested combination.

It is respectfully submitted that none of the references cited by the Examiner discloses, suggests, or renders obvious the method of forming high resolution electronic circuits on a substrate in which the structure including a substrate, a conductive pattern formed thereon, a dielectric layer, and a release layer, is heated to a temperature in a range of approximately 150°C - 175°C to enhance mechanical integrity of the conductive material within the channels formed by the laser ablation in the dielectric layer and in the substrate, and to create permanent adhesion between the conductive material and the upper surface of the substrate where the conductive material is formed, patterned, and

permanently remains. This feature is not presented in any of the references cited by the Examiner, taken singly or in any combination thereof.

Independent Claims 1 and 11 now clearly direct themselves to the concept of heating the substrate, the layer of dielectric film, conductive material in at least one channel, and the release layer to a temperature in a range of approximately 150°C - 175°C to enhance mechanical integrity of the conductive material within the at least one channel and to create permanent adhesion between the conductive material and the upper surface of the substrate, and wherein the electrically conductive material is formed, patterned, and remains permanently on the upper surface of the substrate.

As this feature is now clearly emphasized in Independent Claims 1 and 11, it is believed that Claims 1 and 11, as amended, are patentably distinct from the cited prior art, and the allowance of these Claims 1 and 11 is respectfully requested.

Claims 2-10, and 12-20 are dependent on Claims 1 and 11 respectively. It is believed that these Claims 2-10 and 12-20 each add further limitations that are patentably distinct in addition to being dependent upon what is now believed to be a patentable Independent Claim, and therefore, allowable for at least the same reasons.

For all of the foregoing reasons, it is now believed that the subject Patent Application has been placed in condition for allowance; and such action is respectfully requested.

Respectfully submitted,

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